

## CLAIMS

What is claimed is:

1           1.     A jogging structure for translating wiring connections from points in a first  
2 grid to corresponding points in a second grid in a chip carrier module, the structure  
3 comprising:

4                     a first translation layer, coupled to the first grid, said first translation layer  
5 translating the first grid in an x-axis direction; and

6                     a second translation layer, coupled to said first translation layer, said  
7 second translation layer for translating said wiring connections from the first grid in a y-  
8 axis direction, said y-axis direction being orthogonal to said x-axis direction;

9                     wherein said second translation layer is further coupled to the second grid.

1           2.     The structure of claim 1, wherein:

2                     the points within the first grid have a first pitch, said first pitch being  
3 defined by a first distance between neighboring points in the first grid;

4                     the points within the second grid have a second pitch, said second pitch  
5 being defined by a second distance between neighboring points in the second grid; and  
6                     said second pitch is not an integral multiple of said first pitch.

1           3.     The structure of claim 1, wherein:

2                     said first translation layer further comprises a first plurality of signal  
3 interconnects, said first plurality of signal interconnects each having a jog line elongated  
4 along said x-axis direction; and

5                     said second translation layer further comprises a second plurality of signal  
6 interconnects, said second plurality of signal interconnects each having a jog line  
7 elongated along said y-axis direction.

2                   4.     The structure of claim 3, wherein:  
3                         each of said jog lines in said first plurality of signal interconnects is  
4 disposed between an upper via contact and a lower via contact in said first translation  
5 layer; and  
6                         each of said jog lines in said second plurality of signal interconnects is  
7 disposed between an upper via contact and a lower via contact in said second translation  
8 layer.

1                   5.     The structure of claim 4, wherein:  
2                         each individual upper via contact in said first translation layer is in  
3 electrical communication with a corresponding point in the first grid;  
4                         each individual lower via contact in said first translation layer is in  
5 electrical communication with a corresponding upper via contact in said second  
6 translation layer; and  
7                         each individual lower via contact in said second translation layer is in  
8 electrical communication with a corresponding point in the second grid.  
9 signal via in said first plurality of signal vias are in electrical contact with corresponding  
10 individual signal vias in said second plurality of signal vias.

1                   6.     The structure of claim 5, further comprising:  
2                         a first plurality of power busses in said first translation layer, disposed  
3 along said x-axis direction; and  
4                         a second plurality of power busses in said second translation layer,  
5 disposed in said y-axis direction.

7. The structure of claim 1, wherein:

the first grid comprises a C4 grid; and

the second grid comprises a logic service terminal (LST) grid.

8. A module for an integrated circuit (IC) chip, the module comprising:

a first grid for receiving electrical connections from the IC chip; and

a redistribution layer for fanning said electrical connections received by

said first grid from said first grid to a second grid, said redistribution layer further comprising:

a first translation layer, coupled to said first grid, said first

translation layer translating said first grid in an x-axis direction; and

a second translation layer, coupled to said first translation layer,

said second translation layer for translating said wiring connections from said first grid in a y-axis direction, said y-axis direction being orthogonal to said x-axis direction;

wherein said second translation layer is further coupled to said

second grid.

9. The module of claim 8, wherein:

the points within said first grid have a first pitch, said first pitch being

defined by a first distance between neighboring points in said first grid;

the points within said second grid have a second pitch, said second pitch

being defined by a second distance between neighboring points in said second grid; and

said second pitch is not an integral multiple of said first pitch.

1                   10.    The module of claim 8, wherein:  
2                        said first translation layer further comprises a first plurality of signal  
3 interconnects, said first plurality of signal interconnects each having a jog line elongated  
4 along said x-axis direction; and  
5                        said second translation layer further comprises a second plurality of signal  
6 interconnects, said second plurality of signal interconnects each having a jog line  
7 elongated along said y-axis direction.

1                   11.    The module of claim 10, wherein:  
2                        each of said jog lines in said first plurality of signal interconnects is  
3 disposed between an upper via contact and a lower via contact in said first translation  
4 layer; and  
5                        each of said jog lines in said second plurality of signal interconnects is  
6 disposed between an upper via contact and a lower via contact in said second translation  
7 layer.

1                   12.    The module of claim 11, wherein:  
2                        each individual upper via contact in said first translation layer is in  
3 electrical communication with a corresponding point in the first grid;  
4                        each individual lower via contact in said first translation layer is in  
5 electrical communication with a corresponding upper via contact in said second  
6 translation layer; and  
7                        each individual lower via contact in said second translation layer is in  
8 electrical communication with a corresponding point in the second grid.

1                   13.     The module of claim 12, further comprising:  
2                         a first plurality of power busses in said first translation layer, disposed  
3                   along said x-axis direction; and  
4                         a second plurality of power busses in said second translation layer,  
5                   disposed in said y-axis direction.

1                   14.     The module of claim 8, wherein:  
2                         said first grid comprises a C4 grid; and  
3                         said second grid comprises a logic service terminal (LST) grid.

1                   15.     A method for implementing a wiring translation in chip carrier module  
2                   between corresponding points in a first grid and a second grid, the points in the first grid  
3                   defining a first plane and the points in the second grid defining a second plane, the second  
4                   plane lying substantially parallel to the first plane, the method comprising:  
5                         connecting the first grid to a first translation layer within the module, said  
6                   first translation layer translating the points in the first grid in a first direction; and  
7                         connecting a second translation layer between said first translation layer  
8                   and the second grid, said second translation layer translating the points in the first grid in  
9                   a second direction, said second direction being orthogonal to said first direction.

1 16. The method of claim 15, wherein:  
2 said first translation layer is configured to include a first plurality of signal  
3 interconnects, said first plurality of signal interconnects each having a jog line elongated  
4 along said x-axis direction; and  
5 said second translation layer is configured to include a second plurality of  
6 signal interconnects, said second plurality of signal interconnects each having a jog line  
7 elongated along said y-axis direction.

1 17. The method of claim 16, wherein:  
2 each of said jog lines in said first plurality of signal interconnects is  
3 disposed between an upper via contact and a lower via contact in said first translation  
4 layer; and  
5 each of said jog lines in said second plurality of signal interconnects is  
6 disposed between an upper via contact and a lower via contact in said second translation  
7 layer.

1 18. The method of claim 17, wherein:  
2 each individual upper via contact in said first translation layer is in  
3 electrical communication with a corresponding point in the first grid;  
4 each individual lower via contact in said first translation layer is in  
5 electrical communication with a corresponding upper via contact in said second  
6 translation layer; and  
7 each individual lower via contact in said second translation layer is in  
8 electrical communication with a corresponding point in the second grid.  
9 signal via in said first plurality of signal vias are in electrical contact with corresponding  
10 individual signal vias in said second plurality of signal vias.

